LANSDALE Semiconductor, Inc.

ML12040 Phase–Frequency Detector

Legacy Device: *Motorola MC12040*

The ML12040 is a phase–frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the ML12149), it is useful in a broad range of phase–locked loop applications.

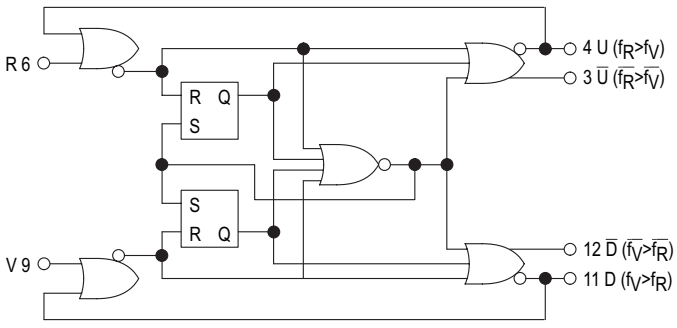
- Operating Frequency = 80 MHz Typical
- Operating Temperature Range T_A = 0° to 75°C

Pin Conversion Table

14 Pin DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14
20 Pin PLCC	2	3	4	6	8	9	10	12	13	14	16	18	19	20

Inputs		Outputs			
R	**V**	**U**	**D**	$\overline{\text{U}}$	$\overline{\text{D}}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1

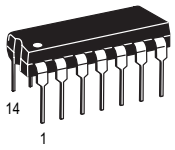
LOGIC DIAGRAM



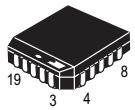
V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{EE} = Pin 7

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.



P DIP 14 = CP
PLASTIC PACKAGE
CASE 646



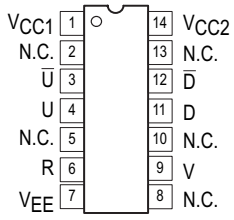
PLCC 20 = -4P
PLASTIC PACKAGE
CASE 775

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 14	MC12040P	ML12040CP
PLCC 20	MC12040FN	ML12040-4P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

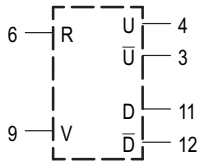
PIN CONNECTIONS



(Top View)

ELECTRICAL CHARACTERISTICS

The ML12040 has been designed to meet the DC specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 Ω resistor to 3.0 V for 5.0 V tests and through a 50 Ω resistor to –2.0 V for –5.2 V tests.



NOTE: For more information on using an ECL device in a 5.0 V system, refer to Application Note AN1406/D, "Designing with PECL (ECL at 5.0 V)"

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
0 C	–0.840	–1.870	–1.145	–1.490	–5.2
25 C	–0.810	–1.850	–1.105	–1.475	–5.2
75 C	–0.720	–1.830	–1.045	–1.450	–5.2

Supply Voltage = –5.2V

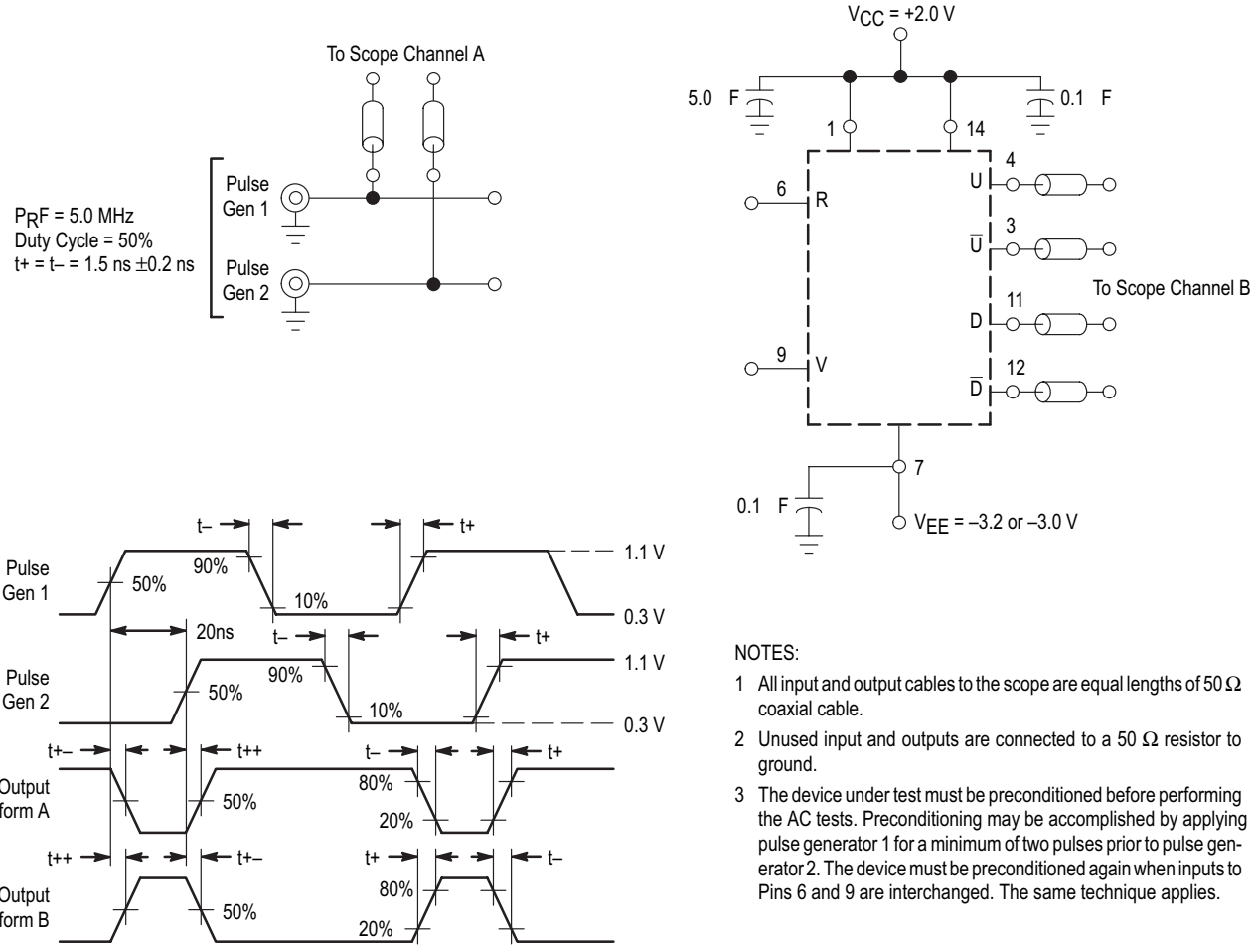
Symbol	Characteristics	Pin Under Test	MC12040 0 C Min	MC12040 0 C Max	MC12040 25 C Min	MC12040 25 C Max	MC12040 75 C Min	MC12040 75 C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
I_E	Power Supply Drain	7			–120	–60			mAdc					7	1,14
I_{INH}	Input Current	6 9				350 350			Adc	6 9				7 7	1,14 1,14
V_{OH}[1]	Logic "1" Output Voltage	3 4 11 12	–1.000	–0.840	–0.960	–0.810	–0.900	–0.720	Vdc					7	1,14
V_{OL}[1]	Logic "0" Output Voltage	3 4 11 12	–1.870	–1.635	–1.850	–1.620	–1.830	–1.595	Vdc					7	1,14
V_{OHA}[2]	Logic "1" Input Voltage	3 4 11 12	–1.020		–0.980		–0.920		Vdc			6.9		7	1,14
V_{OLA}[2]	Logic "0" Input Voltage	3 4 11 12		–1.615		–1.600		–1.575	Vdc			9 6 9 6	6 9 6 9	7	1,14

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
0 C	+4.160	+3.130	+3.855	+3.510	+5.0
25 C	+4.190	+3.150	+3.895	+3.525	+5.0
75 C	+4.280	+3.170	+3.955	+3.550	+5.0

Supply Voltage = +5.0V

Symbol	Characteristics	Pin Under Test	MC12040 0 C Min	MC12040 0 C Max	MC12040 25 C Min	MC12040 25 C Max	MC12040 75 C Min	MC12040 75 C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
I_E	Power Supply Drain	7			–115	–60			mAdc					1,14	7
I_{INH}	Input Current	6 9				350 350			Adc	6 9				1,14 1,14	7 7
V_{OH}[1]	Logic "1" Output Voltage	3 4 11 12	4.000	4.160	4.040	4.190	4.100	4.280	Vdc					1,14	7
V_{OL}[1]	Logic "0" Output Voltage	3 4 11 12	3.190	3.430	3.210	3.440	3.230	3.470	Vdc					1,14	7
V_{OHA}[2]	Logic "1" Input Voltage	3 4 11 12	3.980		4.020		4.080		Vdc			6.9		1,14	7
V_{OLA}[2]	Logic "0" Input Voltage	3 4 11 12		3.450		3.460		3.490	Vdc			9 6 9 6	6 9 6 9	1,14	7

Figure 1. AC Tests



NOTES:

1 All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

2 Unused input and outputs are connected to a 50 Ω resistor to ground.

3 The device under test must be preconditioned before performing the AC tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to Pins 6 and 9 are interchanged. The same technique applies.

Symbol	Characteristic	Pin Under Test	Output Waveform	ML12040 0 C Max	ML12040 25 C Max	ML12040 85 C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED: Pulse Gen 1	Pulse Gen 2	V_{EE} –3.0 or –3.2 V	V_{CC} 2.0 V
t_{6+4+}	Propagation Delay	6,4	B	4.6	4.6	5.0	ns	6	9	7	1,14
t_{6+12+}		6,12	A	6.0	6.0	6.6		9	6		
$t_{6+3–}$		6,3	A	4.5	4.5	4.9		6	9		
$t_{6+11–}$		6,11	B	6.4	6.4	7.0		9	6		
t_{9+11+}		9,11	B	4.6	4.6	5.0		9	6		
t_{9+3+}		9,3	A	6.0	6.0	6.6		6	9		
$t_{9+12–}$		9,12	A	4.5	4.5	4.9		9	6		
$t_{9+4–}$		9,4	B	6.4	6.4	7.0		6	9		
t_{3+}	Output Rise Time	3	A	3.4	3.4	3.8	ns	6	9	7	1,14
t_{4+}		4	B					6	9		
t_{11+}		11	B					9	6		
t_{14+}		14	A					9	6		
$t_{3–}$	Output Fall Time	3	A	3.4	3.4	3.8	ns	6	9	7	1,14
$t_{4–}$		4	B					6	9		
$t_{11–}$		11	B					9	6		
$t_{14–}$		14	A					9	6		

Legacy Applications Information

The ML12040 is a logic network designed for use as a phase comparator for MECL–compatible input signals. It determines the “lead” or “lag” phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of ±2π radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 2), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (Pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 2), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start–up. A stable phase–locked loop will result from either condition.

Phase error information is contained in the output duty cycle that is, the ratio of the output pulse width to total period. By integrating or low–pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage controlled oscillator can be developed. A circuit useful for this function is shown in Figure 3.

Proper level shifting is accomplished by differentially driving the operational amplifier from the normally high outputs of the phase detector (U and D). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched “1” levels from the phase detector). The U and D outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R–C filtering imbedded within the input network (Figure 3) may be very beneficial since the very narrow correctional pulses of the ML12040 would not normally be integrated by the amplifier. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector “high” states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of 0.016/0.16 = 0.1 radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 3). Phase error over temperature depends on how much the offending parameters drift.

Figure 2. Timing Diagram

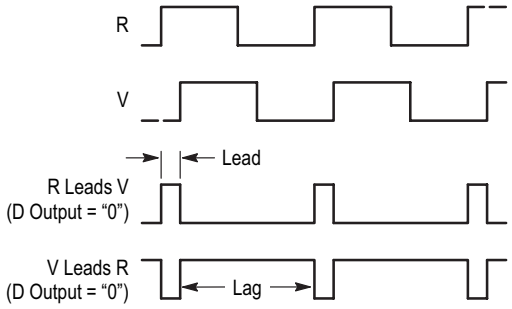
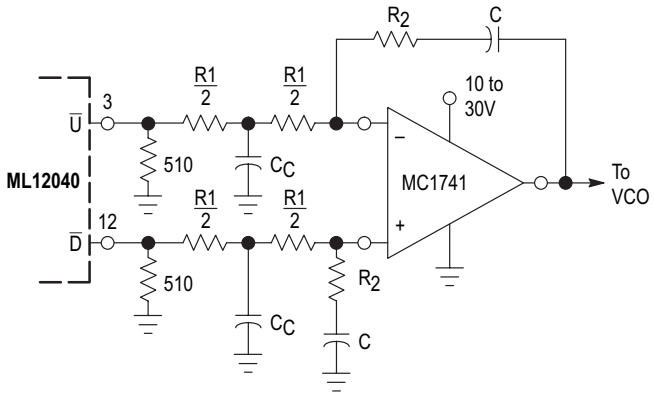
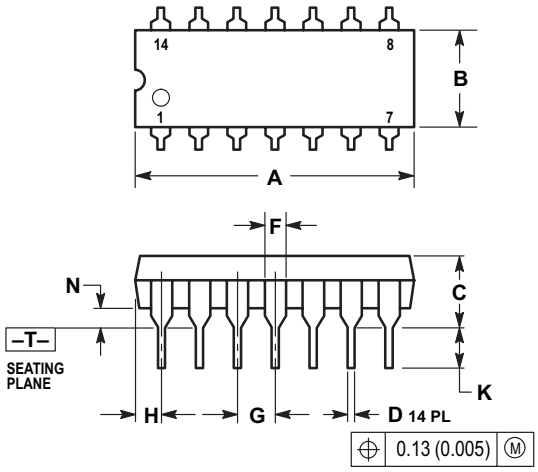


Figure 3. Typical Filter and Summing Network



OUTLINE DIMENSIONS

P DIP 14 = CP
PLASTIC PACKAGE
(ML12040CP)
CASE 646–06
ISSUE M

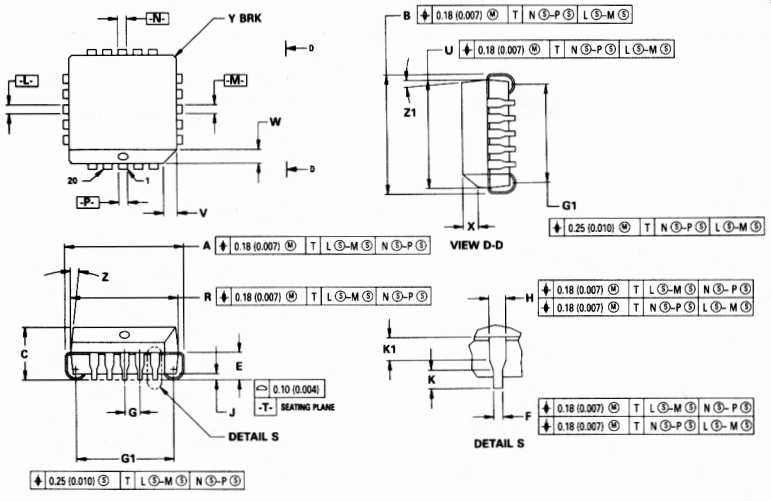


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	—	10°	—	10°
N	0.015	0.039	0.38	1.01

PLCC 20 = -4P
CASE 775-02
Plastic Package
(ML12040-4P)

NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSTION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°